ABSTRACT OF THE DISCLOSURE

A simulation apparatus for simulating a pipeline processor including a pipeline simulation unit and an instruction simulation unit. The simulation apparatus includes a pipeline simulation unit is operable to simulate a group of instructions comprising a plurality of instructions to be executed simultaneously. The instruction simulation unit is operable to simulate a sequential execution, of the group of instructions on an instruction-by-instruction basis, based on the simulation result performed by the pipeline simulation unit. The instruction simulation unit generates the simulation result by undoing the simulation where an instruction included in the group of instructions that has just been simulated by the pipeline simulation unit.